

FQP3P50

P-Channel QFET® MOSFET

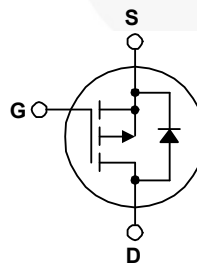
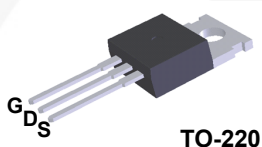
-500 V, -2.7 A, 4.9 Ω

Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -2.7 A, -500 V, $R_{DS(on)} = 4.9 \Omega$ (Max.) @ $V_{GS} = -10 V$, $I_D = -1.35 A$
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ 9.5 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FQP3P50	Unit
V _{DSS}	Drain-Source Voltage	-500	V
I _D	Drain Current - Continuous (T _C = 25°C)	-2.7	A
	Drain Current - Continuous (T _C = 100°C)	-1.71	A
I _{DM}	Drain Current - Pulsed (Note 1)	-10.8	A
V _{GSS}	Gate-Source Voltage	± 30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	250	mJ
I _{AR}	Avalanche Current (Note 1)	-2.7	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	8.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
P _D	Power Dissipation (T _C = 25°C)	85	W
	- Derate above 25°C	0.68	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FQP3P50	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case, Max.	2.4	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

Typical Characteristics

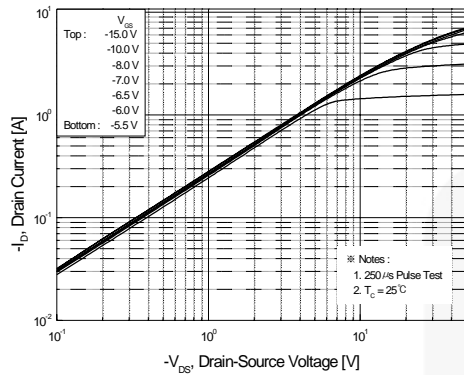


Figure 1. On-Region Characteristics

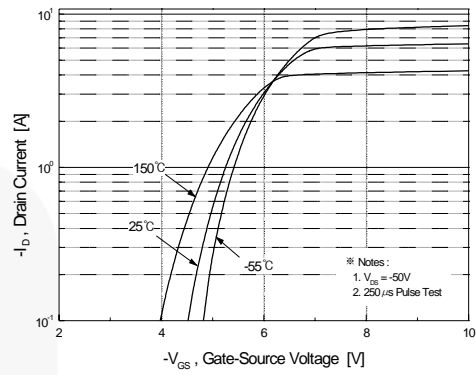


Figure 2. Transfer Characteristics

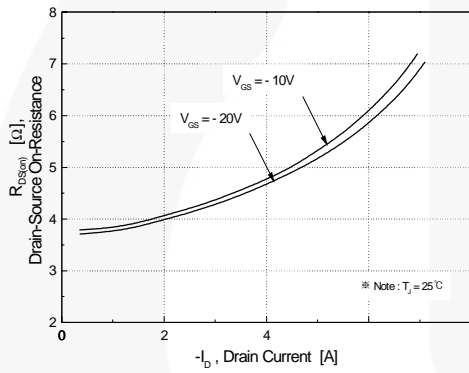


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

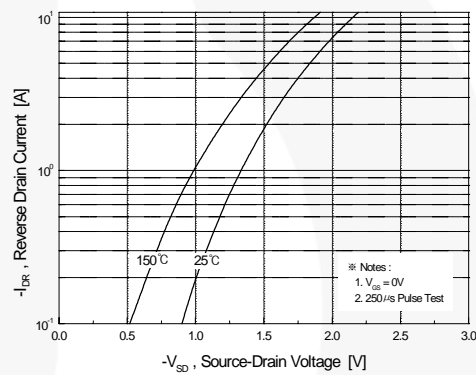


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

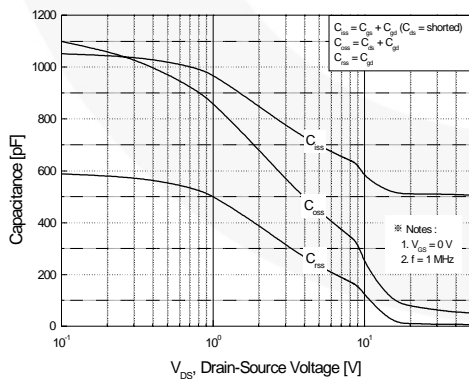


Figure 5. Capacitance Characteristics

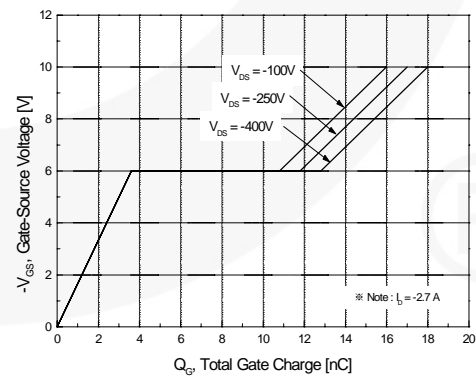


Figure 6. Gate Charge Characteristics

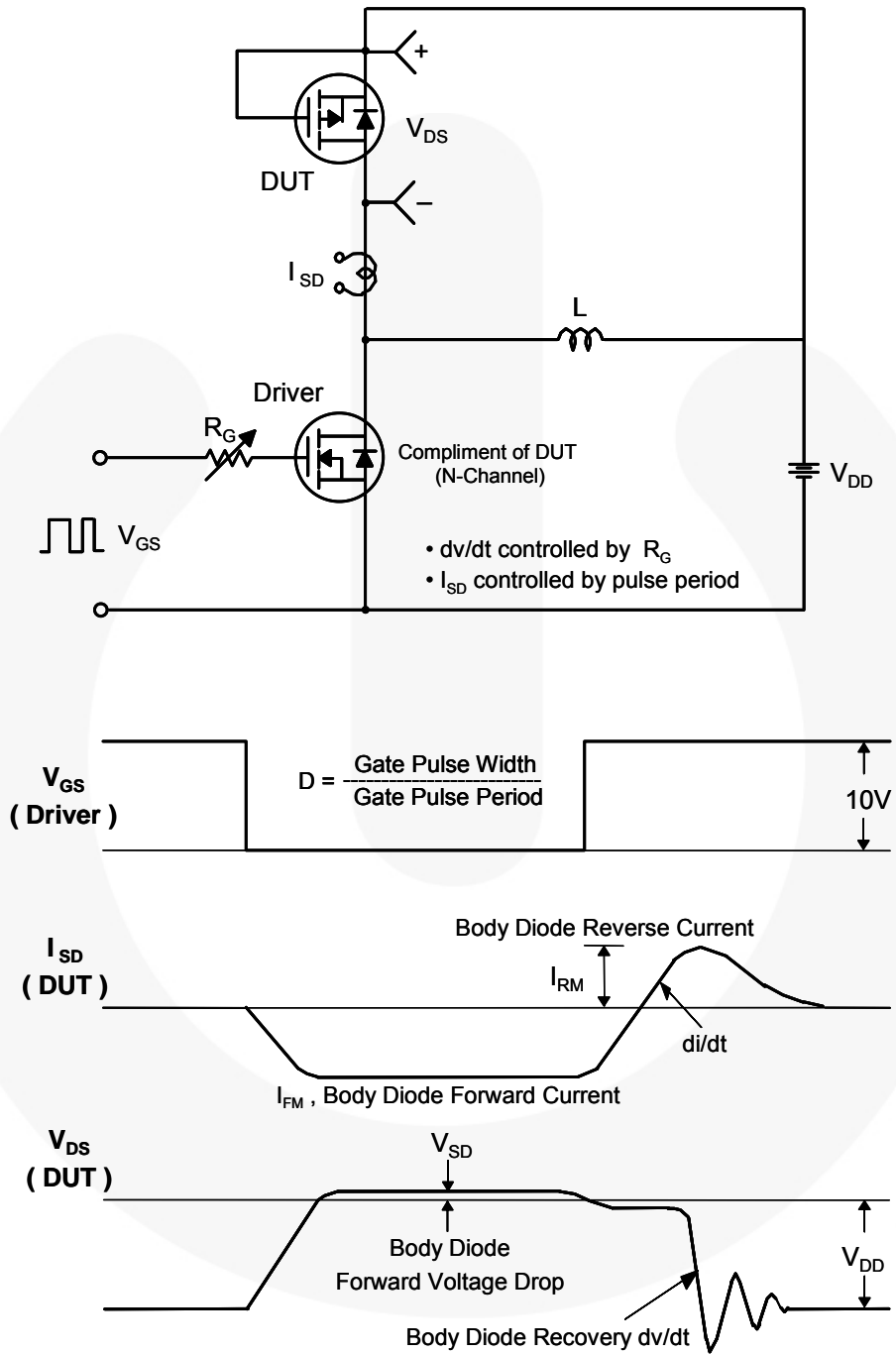


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

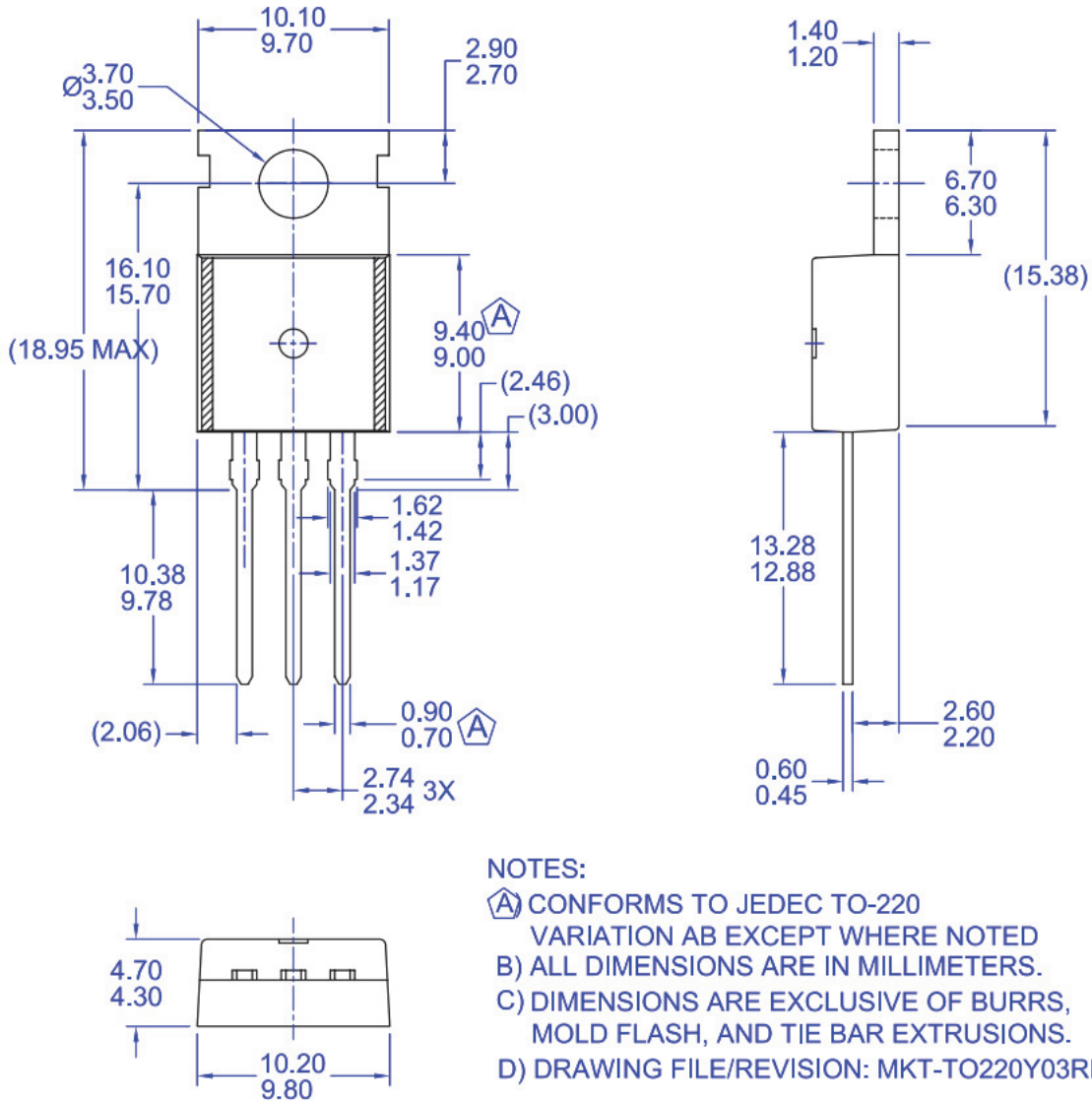


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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